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AND preload OR overlap "floating point regis

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RM Tomasulo - IBM Journal of Research and Development, 1967 - [courses.ece.uiuc.edu](#)

... This sequence illustrates the cardinal precedence principle: No floating-point register may participate ... Now overlap is impossible and the program ...

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[Integrating register allocation and instruction scheduling for RISCs](#)

DG Bradley, SJ Eggers, RR Henry - Proceedings of the fourth international conference on ..., 1991 - [portal.acm.org](#)

... additional register is used, then they can overlap (b). Assuming a 4-cycle multiply, schedule (b) takes 4 fewer cycles. shown. Assuming no cache misses and a 2 ...

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[The MIPS R10000 Superscalar Microprocessor](#) - ► [toronto.edu \(pdf\)](#)

KC Yeager - 1996 - [doi.ieeecomputersociety.org](#)

... single- or double-precision formats in the floating-point register file ... 13 Clocks and output drivers ... secondary-cache data buffer to reduce overlap current spikes ...

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[A pipelined interface for high floating-point performance with precise exceptions.](#)

S Iacobovici - IEEE Micro, 1988 - [doi.ieeecomputersociety.org](#)

... floating-point instruction-execution overlap becomes less ... of floating-point and integer instructions ... instructions with floating-point register destinations. ...

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[The Visual Instruction Set \(VIS\) in UltraSPARCm](#)

L Kohn, G Maturana, M Tremblay, A Prabhu, G Zyner - Proceedings of the 40th IEEE Computer Society International ..., 1995 - [doi.ieeecs.org](#)

... on the enclosing cube into the floating point register file, It assumes 16 bits ... the destination address is aligned to a 64byte boundary, and preload the source ...

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[Developing the WTL 3170/3171 Sparc floating-point coprocessors](#)

M Birman, A Samuels, G Chu, T Chuk, L Hu, J McLeod ... - IEEE Micro, 1990 - [doi.ieeecomputersociety.org](#)

... to integrate all floating-point controller functions; floating-point register file; and ... 170 and 3171 allow a multiply and an add operation to overlap. ...

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[The Alpha 21264 microprocessor architecture](#)

RE Kessler, EJ McLellan, DA Webb - Computer Design: VLSI in Computers and Processors, 1998. ..., 1998 - [ieeexplore.ieee.org](#)

... Floating-Point Register Rename ... prefetch the associated (64-byte) cache blocks to overlap the cache ... can also eliminate unnecessary data reads, and control cache ...

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Key authors: R Tomasulo - K Yeager - R Kessler - E McLellan - D Weaver



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